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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)		**Group Art Unit: 2193**
Joseph H. End III		**Examiner: NGO, CHUONG D**
Serial No.:	**09/971,949**	
Filed:	**October 5, 2001**	**Dkt No.: TN205**
Title:	**CIRCUIT AND METHOD FOR HIGH-SPEED EXECUTION OF MODULO DIVISION**	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
MS Non Fee Amendment

APPEAL BRIEF

Please charge the cost for filing this Appeal Brief and the accompanying Petition for a One-Month Extension of Time to Account No. 19-3790 (a duplicate of this page is enclosed).

Attached is an APPENDIX OF APPEALED claims containing a copy of the appealed claims.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

02/16/2006
Date

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(Signature of person mailing paper)

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Real party in interest

The real party in interest is Unisys Corporation.

Related appeals and interferences

None

State of Amendments

No amendments are pending

Status of claims

The status of the claims in this application is as follows:

Claims 1-14 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tate et al.

Claims 1-14 also stand rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida.

All of claims 1-14 are being appealed.

The appealed claims are set forth in the attached APPENDIX OF APPEALED CLAIMS.

Status of amendments

There are no amendments pending.

Summary of claimed subject matter

Claims 1 and 12 are the only independent claims. The 41.37(c)v) requirements for each is provided below.

Claim 1

Claim 1 is directed to a circuit, such as illustrated in Fig. 2, for calculating and outputting a modulo value resulting from a simulated division of a dividend by a divisor. As explained in the specification, page 1, lines 12-14, a modulo operation is a type of arithmetic division, except rather than returning the quotient resulting from a division by a divisor, the modulo operation returns the remainder resulting from that division. This remainder in the desired modulo value.

As defined in claim 1 (and explained in the specification, page 7, line 11 to page 9, line 7), a plurality of subtraction circuits (12a – 12f in Fig. 2) receive a common dividend signal (at input B in Fig. 2) and at least one respective test value signal (TV0-TV6 at input B) representing an integer multiple of the divisor. Each subtraction circuit (12a – 12f in Fig. 2) subtracts its respective test value signal to produce a respective remainder signal (13a – 13g in Fig. 2) and also a respective carry/borrow signal (CYBR1 – CYBR6). Logic (Remainder Selection Logic 16 in Fig. 2) use these carry/borrow signals to determine which of the remainder signals represents a true remainder (21) of the division of the dividend by the divisor.

Claim 4

Claim 4 recites that the respective test value signals are hard coded in the circuit (see support in specification 1, page 8, lines 10-11). This is possible in the preferred embodiment since the divisor is a constant. Thus, the respective test values can be built into the logic so as to be immediately available at the respective test value inputs of the subtraction circuits without the need for any processing or other calculations during the division operation.

Claim 5 and 6

These claims are based on the embodiment of Fig. 2A (see specification, page 12, line 9 to page 13, line 7) wherein the number of subtraction circuits required is reduced by reusing the subtraction circuits during a second subtraction cycle in order to perform the required number of subtractions for all of the test values.

Claim 7

This claim is directed to a SEQUENCE CONTROLLER (25 in Fig. 2A) which controls the input of the first and second subsets of test value signals to the subtraction circuits during the respective first and second subtraction cycles.

Claim 8

This claim requires that a variable dividend have a value ranging from 0 to 65535 inclusive and that the divisor comprises a fixed value of 9973.

Claim 12

Claim 12 basically defines the same invention as claim 1, except in method format. Accordingly, reference is directed to the 41.37(c)(v) description provided for claim 1.

Claim 13

See the discussion regarding claim 8.

Claim 14

See the discussion regarding claims 5 and 6.

Grounds of rejection to be reviewed on appeal

(1) Rejection of claims 1-14 under 35 U.S.C. 102(b) as being anticipated by Tate et al.

(2) Rejection of claims 1-14 under 35 U.S.C. 102(b) as being anticipated by Yoshida.

Argument

Initially, the applicable law regarding 35 USC 102(b) rejections will be briefly summarized.

It is well established that "A claim is anticipated under 35 U.S.C. 102(b) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior at reference." Verdegaal Bros. V. Union Oil Co. of California, 814 F2d 628, 631 2 USPQ 2d1051, 1053 (Fed. Cir. 1987) (see also MPEP 2131).

Additionally, with regard to inherency, it was held in the CAFC decision, Trintec Industries, Inc. v. Top-U.S.A. Corp. (CAFC 7/2/02) that "Inherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art." In re Robertson, 169, F. 3d 743, 745, 49 USPQ 2d 1949, 1950-51 (Fed. Cir. 1999).

Still further, the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijackaert, 9F.3d, 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. Ap. & Inter. 1990) (emphasis in original). (Also see MPEP 2112).

Additionally note the recent CAFC decision, Elan Pharmaceuticals v. Mayo Foundation for Medical Education and Research, 68 USPQ2d 1373 (CAFC, Oct. 2, 2003) which holds that: "The disclosure in an anticipating reference must be adequate to enable the desired subject matter. It is insufficient to name or describe the desired subject matter, if it cannot be produced without undue experimentation."

The 35 U.S.C. 102(b) rejections based on Tate et al and Yoshida will now be specifically considered.

The Tate and Yoshida patents are unquestionably directed to a divider approach whereby the quotient and final remainder value are generated in a manner basically similar to manual long division using successive iterations and partial remainders. Although a final partial remainder is ultimately obtained in the Tate et al. and Yoshida embodiments, it clearly has not been obtained in the manner required by applicant's claims.

Note that independent claim 1 requires that each subtraction circuit subtract the respective test value (representing a respective integer multiple of divisor) from the common dividend signal to produce a respective remainder signal and a respective borrow carry/borrow signal. Logic coupled to receive these corresponding carry/borrow signals then determines which of the remainder signals represents a true remainder of the division by the divisor.

The embodiments disclosed by Tate et al. and Yoshida do not meet the above recitations of claim 1, since the resulting remainder from the first subtraction is a partial remainder which does not represent a true remainder of the division of the dividend by the divisor. Such a true remainder is obtained in the Tate et al. and Yoshida embodiments only after the required number of iterations have been performed.

Regarding the Examiner's comment that Tate et al's and Yoshida's partial remainder would be a final remainder if the dividend and divisor were not greater than 7 times the divisor does not change the fact that Tate

et al. as well as Yoshida are implemented to perform divisions outside of this range. Nowhere does either Tate et al. or Yoshida disclose or teach an implementation or method which provides for only a single iteration.

Regarding claim 4, it is not seen, nor has the examiner shown where either Tate et al or Yoshida disclose or teach that the test value signals are hard coded. The examiner's statement that "Tate and Yoshida can be seen as being hard coded in the circuit when the divisor is kept constant" is not sufficient for anticipation purposes, as will be evident from the 35 U.S.C. 102 discussion provided earlier herein.

Regarding claims 5, 6 and 7, it is not seen where the examiner has made any attempt at all to show how these claims are met by the cited references. Applicant therefore submits that, since no basis for anticipation has been made with respect to these claims, the examiner's rejection thereof is not supportable.

Regarding claim 8, the recitation requiring the dividend to be "a variable dividend having a value ranging from 0 to 65535 inclusive, and wherein the divisor comprises a fixed value of 9973" is not merely an intended field of use as alleged by the examiner on page 3 of the Final Action. Rather, this is a proper limitation on the claimed implementation which is not taught by either Tate et al. or Yoshida.

Regarding claims 12, 13 and 14, see the arguments above made for claims 1, 8 and 5-7, respectively.

Conclusion

In view of the foregoing, appellant respectfully submits that the examiner's rejections of the appealed claims are in error. Reversal of these rejections is therefore respectfully solicited.

Respectfully Submitted,
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APPENDIX OF APPEALED CLAIMS

1. A circuit for calculating and outputting a modulo value resulting from a simulated division of a dividend by a divisor, the circuit comprising:

a plurality of subtraction circuits, each one of the subtraction circuits receiving as a first input a common dividend signal representing the dividend and, as a second input, at least one respective test value signal representing a respective integer multiple of the divisor, each one of the subtraction circuits subtracting the respective test value signal input to the subtraction circuit from the common dividend signal to produce a respective remainder signal and a respective carry/borrow signal; and

logic coupled to receive each of the corresponding carry/borrow signals and to determine therefrom which of the remainder signals represents a true remainder of the division of the dividend by the divisor.

2. The circuit recited in claim 1, further comprising a multiplexer that receives each of the remainder signals and, in response to a signal from said logic, outputs the remainder signal representing the true remainder of the division operation.

3. The circuit of claim 1, wherein the plurality of subtraction circuits execute the respective subtraction operations substantially simultaneously.

4. The circuit of claim 1, wherein the respective test value signals are hard coded in the circuit.

5. The circuit of claim 1, wherein each one of the subtraction circuits receives as its second input, at least a further test value signal

representing a further integer multiple of the divisor, and wherein each one of the subtraction circuits subtracts the test value signal from the dividend signal during a first subtraction operation and subtracts the further test value signal from the dividend signal during a second subtraction operation.

6. The circuit of claim 1, wherein the plurality of subtraction circuits is used during a first subtraction cycle to perform respective subtractions using a first subset of respective test value signals, and wherein the plurality of subtraction circuits is then reused during a second subtraction cycle to perform respective subtractions using a second subset of respective test value signals.

7. The circuit recited in claim 6, further comprising a sequence controller that controls the input of the first and second subsets of test value signals to the subtraction circuits during the respective first and second subtraction cycles.

8. The circuit recited in claim 1, wherein the dividend comprises a variable dividend having a value ranging from 0 to 65535 inclusive, and wherein the divisor comprises a fixed value of 9973.

9. The circuit recited in claim 1, wherein each subtraction circuit comprises an adder that receives as its first input the common dividend signal and as its second input a two's complement form of said at least one respective test value signal, and wherein each adder performs its respective subtraction operation using two's complement arithmetic.

10. The circuit recited in claim 1, wherein the respective test value signals are available as inputs to each subtraction circuit prior to each subtraction circuit receiving said common dividend signal.

11. The circuit recited in claim 1, wherein the respective test value signals are available as inputs to each subtraction circuit substantially simultaneously with each subtraction circuit receiving said common dividend signal.

12. A method performed by data processing apparatus for calculating and outputting a modulo value resulting from a simulated division of a dividend by a divisor, the method comprising:

providing a plurality of test value signals each representing a different integer multiple of the divisor, each test value signal corresponding to a different one of the possible quotients that can result from the division of the dividend by the divisor;

separately subtracting each test value signal from the dividend, at least some of the subtractions being performed substantially simultaneously, to produce a respective plurality of possible remainder values and a respective plurality of carry/borrow signals; and

determining from the plurality of carry/borrow signals which of the respective plurality of possible remainder values is the correct remainder value.

13. The method recited in claim 12, wherein the dividend comprises a variable dividend having a value ranging from 0 to 65535 inclusive, and wherein the divisor comprises a fixed value of 9973.

14. The method recited in claim 12, further comprising performing said providing and subtracting steps with a first subset of test

value signals, and thereafter, repeating said providing and subtracting steps with a second subset of test value signals.